LH538600A

CMOS 8M (1M × 8/512K × 16)
High-Speed Mask-Programmable ROM

FEATURES

- 1,048,576 words × 8 bit organization
  (Byte mode)
  524,288 words × 16 bit organization
  (Word mode)
- $\overline{\text{BYTE}}$ input pin selects bit configuration
- Access time: 100 ns (MAX.)
- Power consumption:
  Operating: 550 mW (MAX.)
  Standby: 550 µW (MAX.)
- Static operation
- TTL compatible I/O
- Three-state output
- Single +5 V power supply
- Packages:
  42-pin, 600-mil DIP
  44-pin, 600-mil SOP
  48-pin, 12 × 18 mm^2 TSOP (Type I)

DESCRIPTION

The LH538600A is a CMOS 8M-bit mask-programmable ROM organized as 1,048,576 × 8 bits (Byte mode) or 524,288 × 16 bits (Word mode) that can be selected by $\overline{\text{BYTE}}$ input pin. Due to its high-speed access of 100 ns, it is suited to high-speed laser printers, quality sound electronic musical instruments, etc.

PIN CONNECTIONS

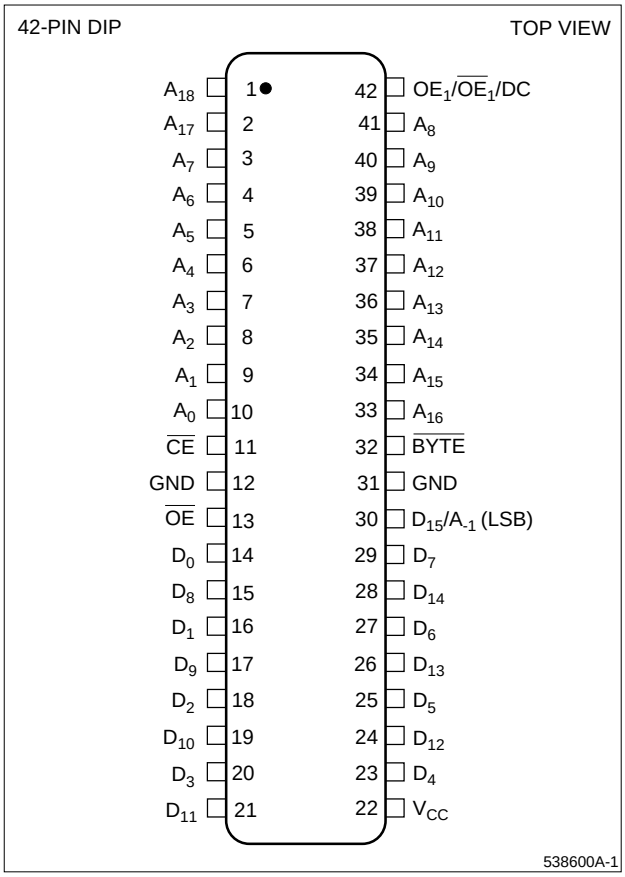


Figure 1. Pin Connections for DIP Package

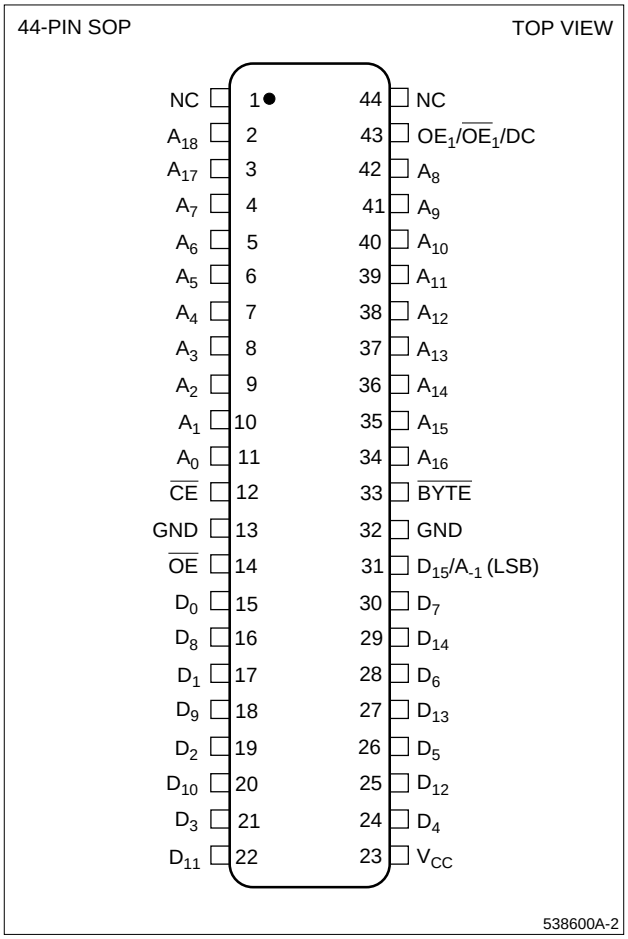


Figure 2. Pin Connections for SOP Package

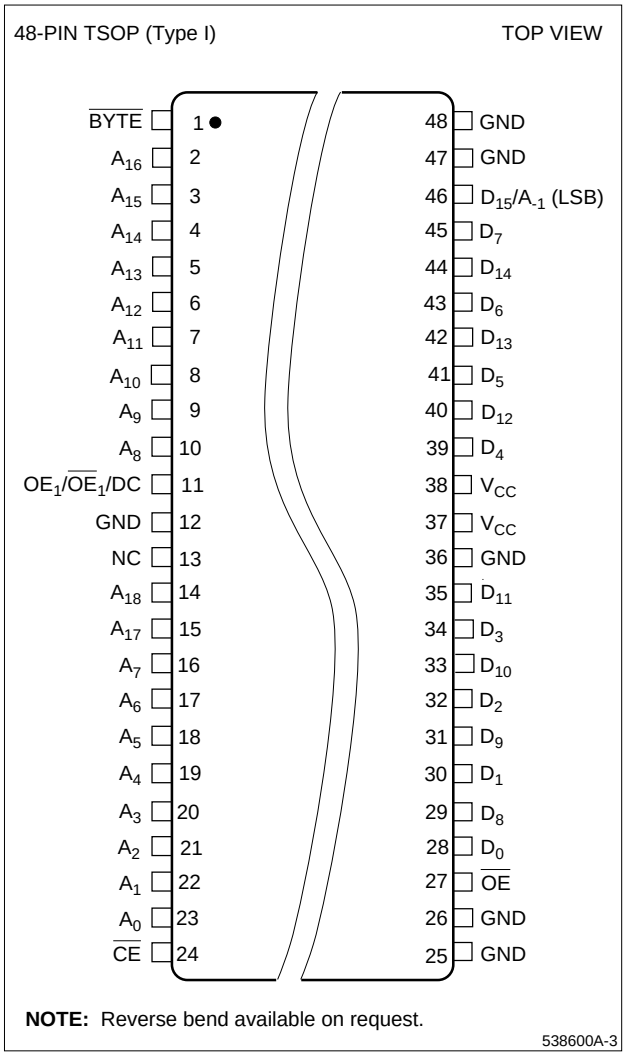


Figure 3. Pin Connections for TSOP Package

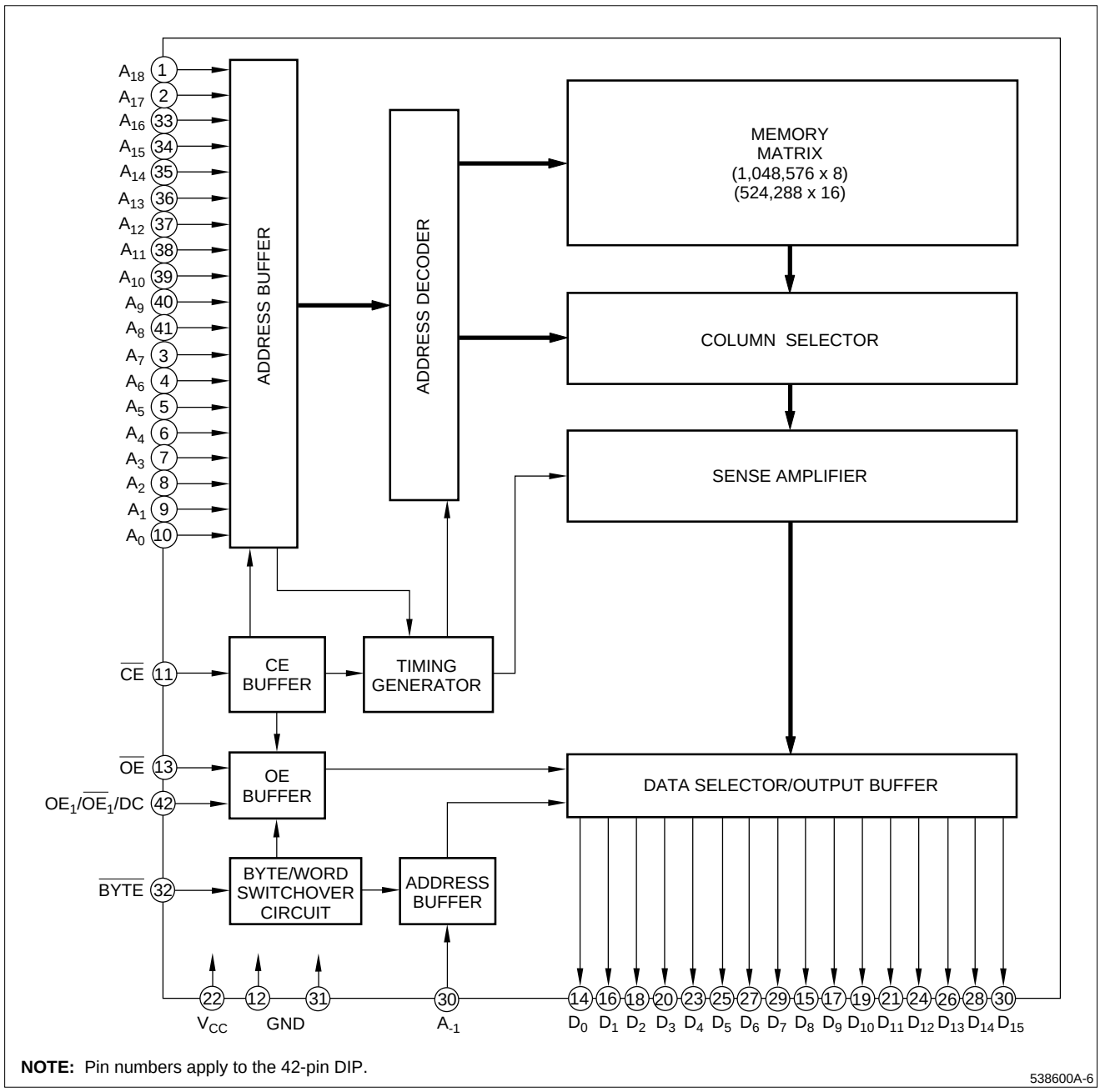


Figure 4. LH538600A Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_{-1}	Address input (BYTE mode)	1
$A_0 - A_{18}$	Address input	
$D_0 - D_{15}$	Data output	1
$\overline{BYTE}$	Byte/word mode switch	1
$\overline{CE}$	Chip enable input	

SIGNAL	PIN NAME	NOTE
$\overline{OE}$	Output enable input	
$OE_1/\overline{OE_1}/DC$	Output enable input	2, 3
V_{CC}	Power supply (+5 V)	
GND	Ground	

NOTES:

1. D_{15}/A_{-1} pin becomes LSB address input (A_{-1}) when the bit configuration is set in byte mode, and data output (D_{15}) when in word mode. The $\overline{BYTE}$ input pin selects bit configuration.
2. An active level of $OE_1/\overline{OE_1}/DC$ is mask-programmable.
3. DC = Don't care.

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$OE_1/\overline{OE_1}$	$\overline{BYTE}$	A_{-1} (D_{15})	DATA OUTPUT		MODE	ADDRESS INPUT		SUPPLY CURRENT
					$D_0 – D_7$	$D_8 – D_{15}$		LSB	MSB	
H	X	X	X	X	High-Z	High-Z	–	–	–	Standby
L	H	L/H	X	X	High-Z	High-Z		–	–	Operating
L	L	H/L	H	Inhibit	$D_0 – D_7$	$D_8 – D_{15}$	16-bit	A_0	A_{18}	Operating
L	L	H/L	L	L	$D_0 – D_7$	High-Z	8-bit	A_{-1}	A_{18}	Operating
L	L	H/L	L	H	$D_8 – D_{15}$	High-Z	8-bit	A_{-1}	A_{18}	Operating

NOTE:
X = H or L, High-Z = High-impedance

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V_{CC}	–0.3 to +7.0	V
Input voltage	V_{IN}	–0.3 to V_{CC} + 0.3	V
Output voltage	V_{OUT}	–0.3 to V_{CC} + 0.3	V
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to + 70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Input 'High' voltage	V_{IH}		2.2	V_{CC} + 0.3	V	
Input 'Low' voltage	V_{IL}		–0.3	0.8	V	
Output 'High' voltage	V_{OH}	I_{OH} = –400 µA	2.4		V	
Output 'Low' voltage	V_{OL}	I_{OL} = 2.0 mA		0.4	V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN}= 0 V, V_{CC}		10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V, V_{CC}		10	µA	1
Operating current	I_{CC1}	t_{RC} = 100 ns		100	mA	2
	I_{CC2}	t_{RC} = 1 µs		90	mA	2
	I_{CC3}	t_{RC} = 100 ns		95	mA	3
	I_{CC4}	t_{RC} = 1 µs		85	mA	3
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}		3	mA	
	I_{SB2}	$\overline{CE}$ = V_{CC} – 0.2 V		100	µA	
Input capacitance	C_{IN}	f = 1 MHz T_A = 25°C		10	pF	
Output capacitance	C_{OUT}			10	pF	

NOTES:
1. $\overline{CE}/\overline{OE}/\overline{OE_1}$ = V_{IH}, OE_1 = V_{IL}
2. V_{IN} = V_{IH} or V_{IL}, $\overline{CE}$ = V_{IL}, outputs open
3. V_{IN} = (V_{CC} – 0.2 V) or 0.2 V, $\overline{CE}$ = 0.2 V, outputs open

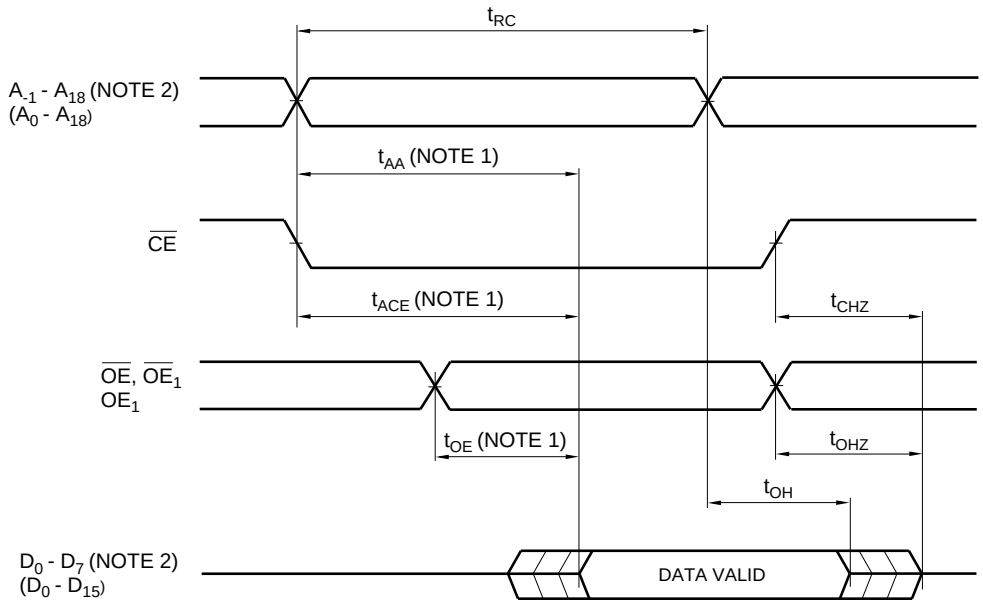
AC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	100		ns	
Address access time	t_{AA}		100	ns	
Chip enable access time	t_{ACE}		100	ns	
Output enable delay time	t_{OE}		50	ns	
Output hold time	t_{OH}	5		ns	
CE to output in High-Z	t_{CHZ}		40	ns	1
OE to output in High-Z	t_{OHZ}		40	ns	

NOTE:
1. This is the time required for the outputs to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 to 2.4 V
Input rise/fall time	10 ns
Input/output reference level	1.5 V
Output load condition	1 TTL + 100 pF



NOTES:
1. Data becomes valid after the intervals t_{AA}, t_{ACE}, and t_{OE} from address input, chip enable, and output enable, respectively, have been met.
2. Applies to byte mode. Signals in parentheses apply to word mode.

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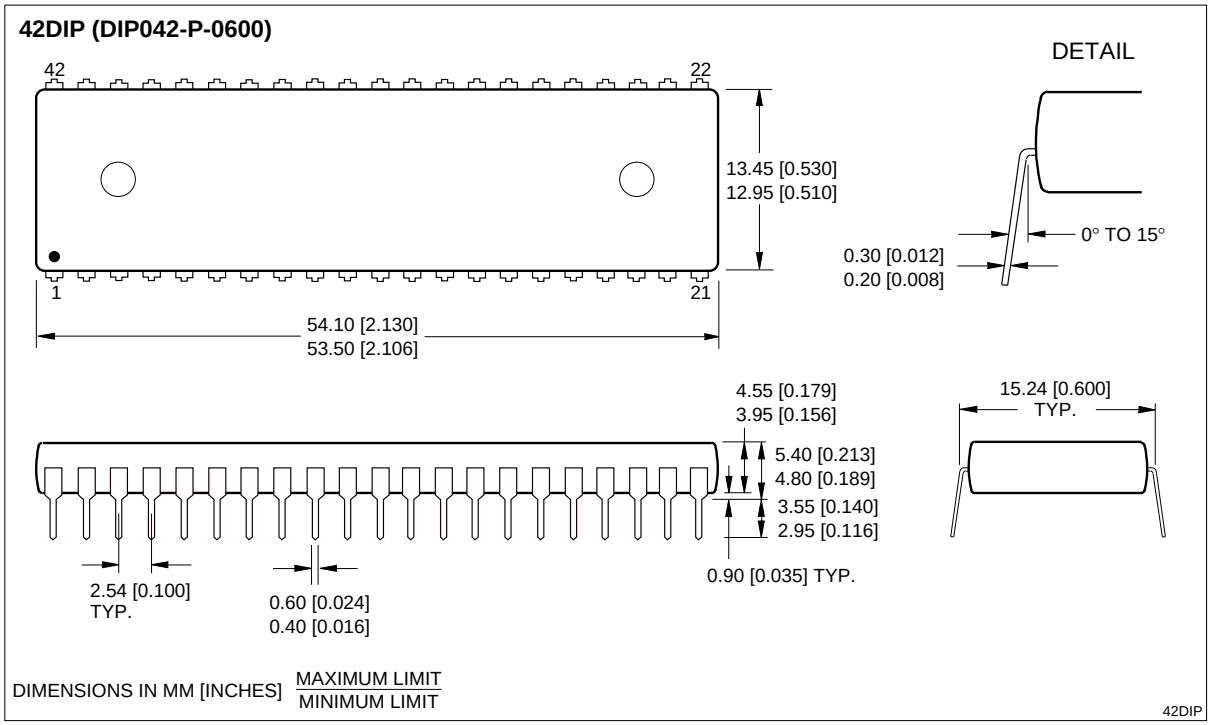
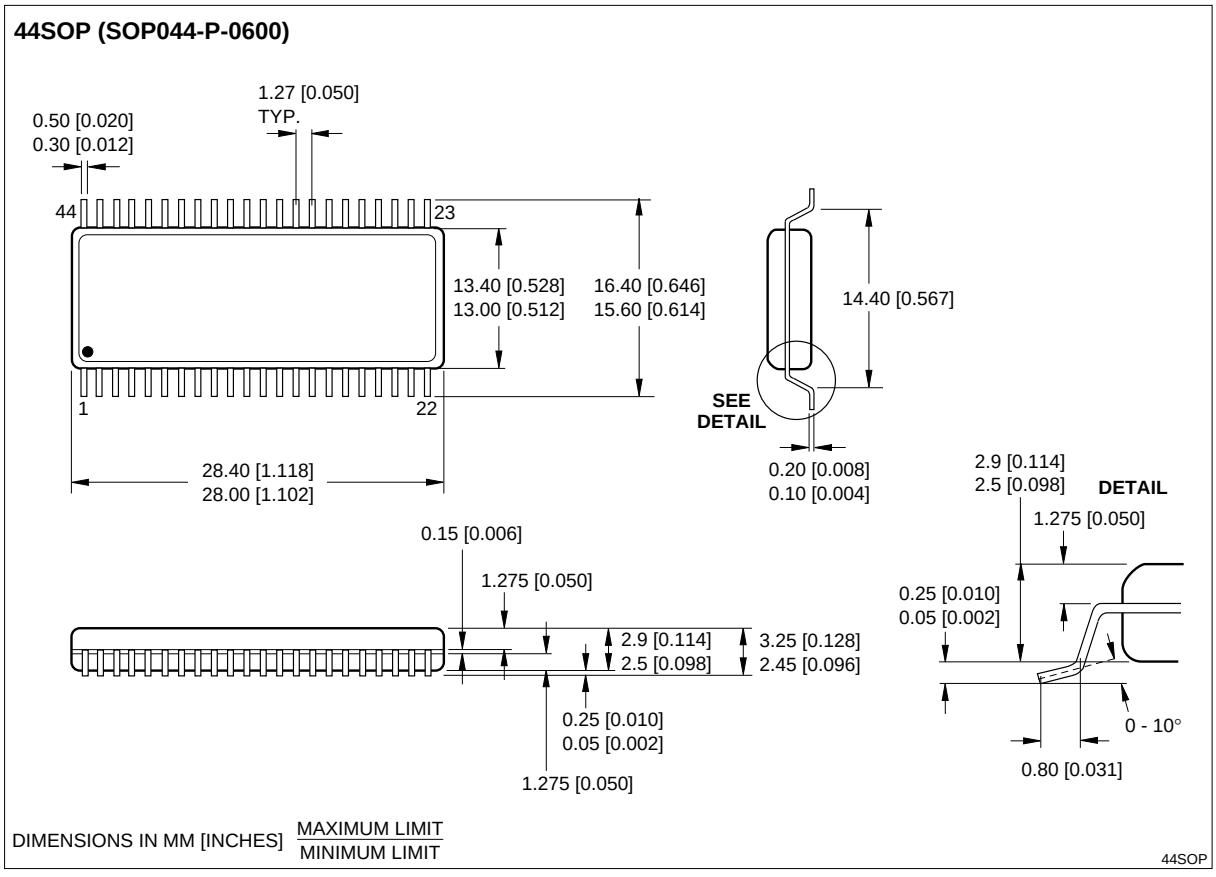
Figure 5. Timing Diagram

PACKAGE DIAGRAMS

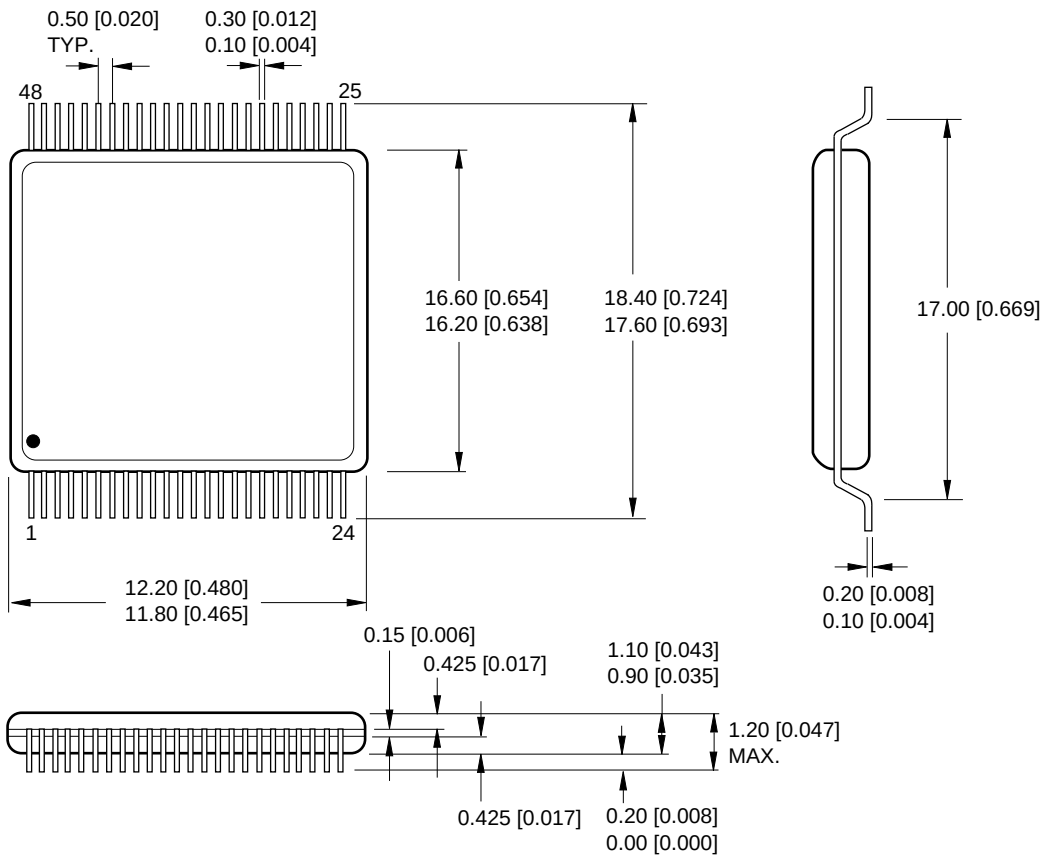


42-pin, 600-mil DIP



44-pin, 600-mil SOP

48TSOP (TSOP048-P-1218)



48-pin, 12 × 18 mm^2 TSOP (Type I)

ORDERING INFORMATION

LH538600A — Device Type

X — Package

- D 42-pin, 600-mil DIP (DIP042-P-0600)
- N 44-pin, 600-mil SOP (SOP044-P-0600)
- T 48-pin, 12 x 18 mm^2 TSOP (Type I) (TSOP048-P-1218)
- TR 48-pin, 12 x 18 mm^2 TSOP (Type I) Reverse bend (TSOP048-P-1218)

CMOS 8M (1M x 8 or 512K x 16) High-Speed Mask-Programmable ROM

Example: LH538600AD (CMOS 8M (1M x 8 or 512K x 16) High-Speed Mask-Programmable ROM, 42-pin, 600-mil DIP)

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